FIG. 1

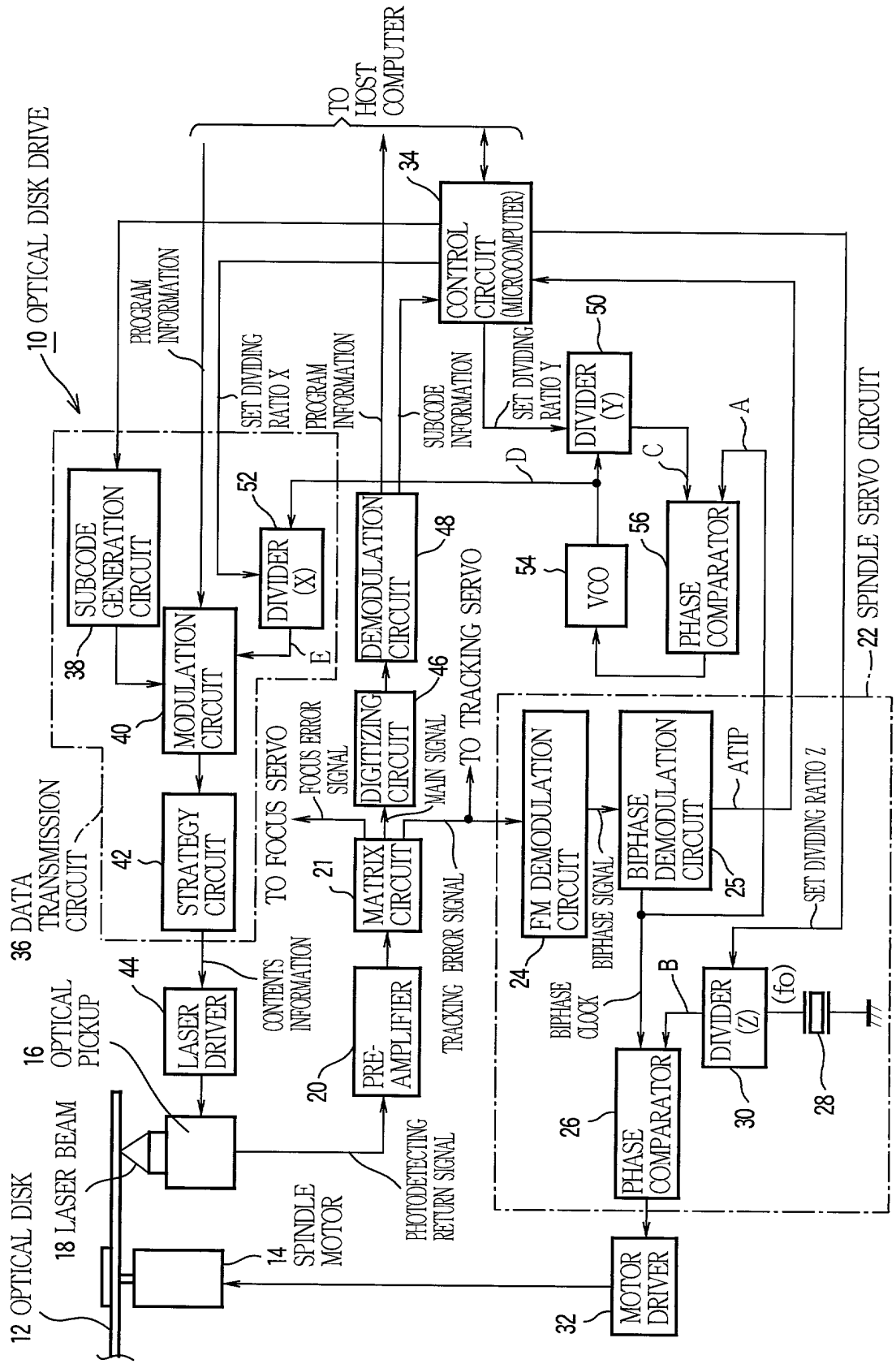
10 OPTICAL DISK DRIVE
TO HOST COMPUTER
34 CONTROL CIRCUIT (MICROCOMPUTER)
PROGRAM INFORMATION
SET DIVIDING RATIO X
PROGRAM INFORMATION
SUBCODE INFORMATION
SET DIVIDING RATIO Y
50 DIVIDER (Y)
A
C
D
52 DIVIDER (X)
E
SUBCODE GENERATION CIRCUIT
38
MODULATION CIRCUIT
40
DEMODULATION CIRCUIT
48
54 VCO
56 PHASE COMPARATOR
22 SPINDLE SERVO CIRCUIT
36 DATA TRANSMISSION CIRCUIT
42 STRATEGY CIRCUIT
TO FOCUS SERVO
FOCUS ERROR SIGNAL
DIGITIZING CIRCUIT
46
MAIN SIGNAL
TO TRACKING SERVO
21 MATRIX CIRCUIT
FM DEMODULATION CIRCUIT
24
BIPHASE SIGNAL
BIPHASE DEMODULATION CIRCUIT
25
ATIP
SET DIVIDING RATIO Z
44 LASER DRIVER
CONTENTS INFORMATION
16 OPTICAL PICKUP
20 PRE-AMPLIFIER
TRACKING ERROR SIGNAL
BIPHASE CLOCK
B
DIVIDER (Z)
(fo)
30
28
12 OPTICAL DISK
18 LASER BEAM
14 SPINDLE MOTOR
PHOTODETECTING RETURN SIGNAL
26 PHASE COMPARATOR
32 MOTOR DRIVER

FIG.2

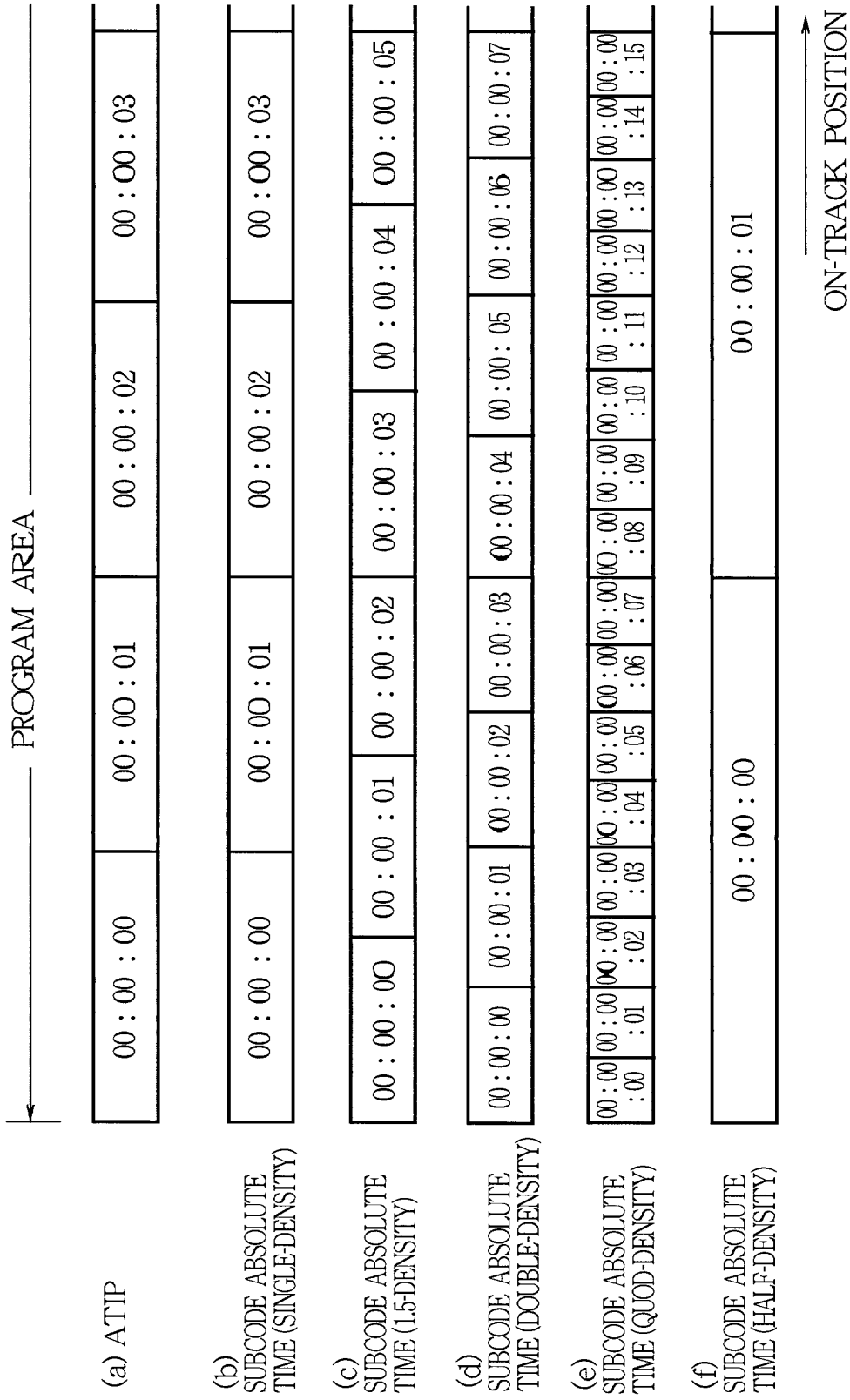
PROGRAM AREA
(a) ATIP
00 : 00 : 00
00 : 00 : 01
00 : 00 : 02
00 : 00 : 03
(b) SUBCODE ABSOLUTE TIME (SINGLE-DENSITY)
00 : 00 : 00
00 : 00 : 01
00 : 00 : 02
00 : 00 : 03
(c) SUBCODE ABSOLUTE TIME (1.5-DENSITY)
00 : 00 : 00
00 : 00 : 01
00 : 00 : 02
00 : 00 : 03
00 : 00 : 04
00 : 00 : 05
(d) SUBCODE ABSOLUTE TIME (DOUBLE-DENSITY)
00 : 00 : 00
00 : 00 : 01
00 : 00 : 02
00 : 00 : 03
00 : 00 : 04
00 : 00 : 05
00 : 00 : 06
00 : 00 : 07
(e) SUBCODE ABSOLUTE TIME (QUOD-DENSITY)
00 : 00 : 00
00 : 00 : 01
00 : 00 : 02
00 : 00 : 03
00 : 00 : 04
00 : 00 : 05
00 : 00 : 06
00 : 00 : 07
00 : 00 : 08
00 : 00 : 09
00 : 00 : 10
00 : 00 : 11
00 : 00 : 12
00 : 00 : 13
00 : 00 : 14
00 : 00 : 15
(f) SUBCODE ABSOLUTE TIME (HALF-DENSITY)
00 : 00 : 00
00 : 00 : 01
ON-TRACK POSITION

FIG.3

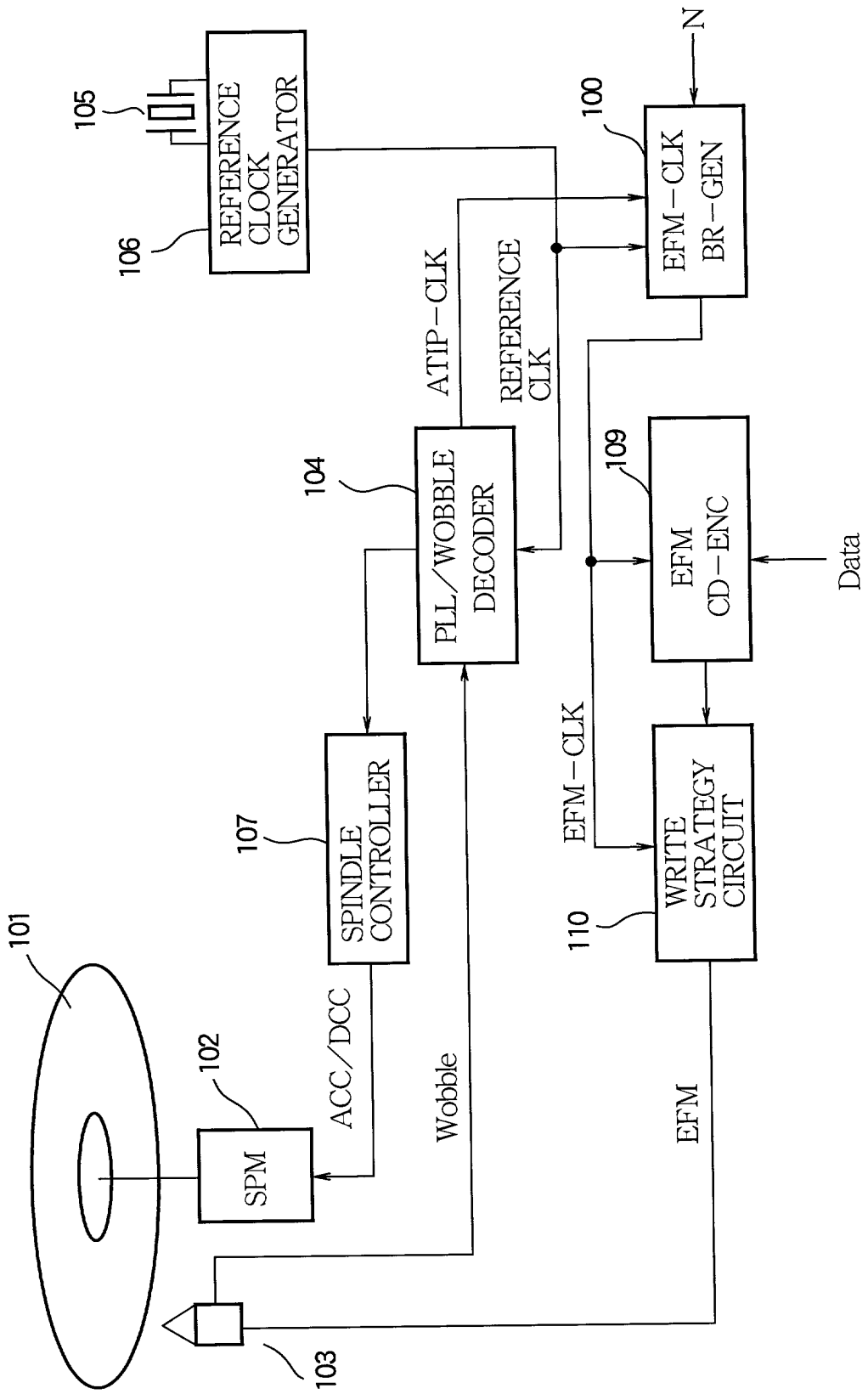
101
102
SPM
103
ACC/DCC
SPINDLE CONTROLLER
107
Wobble
104
PLL/WOBBLE DECODER
ATIP-CLK
REFERENCE CLK
105
106
REFERENCE CLOCK GENERATOR
N
100
EFM-CLK BR-GEN
109
EFM CD-ENC
Data
EFM-CLK
110
WRITE STRATEGY CIRCUIT
EFM

FIG.4

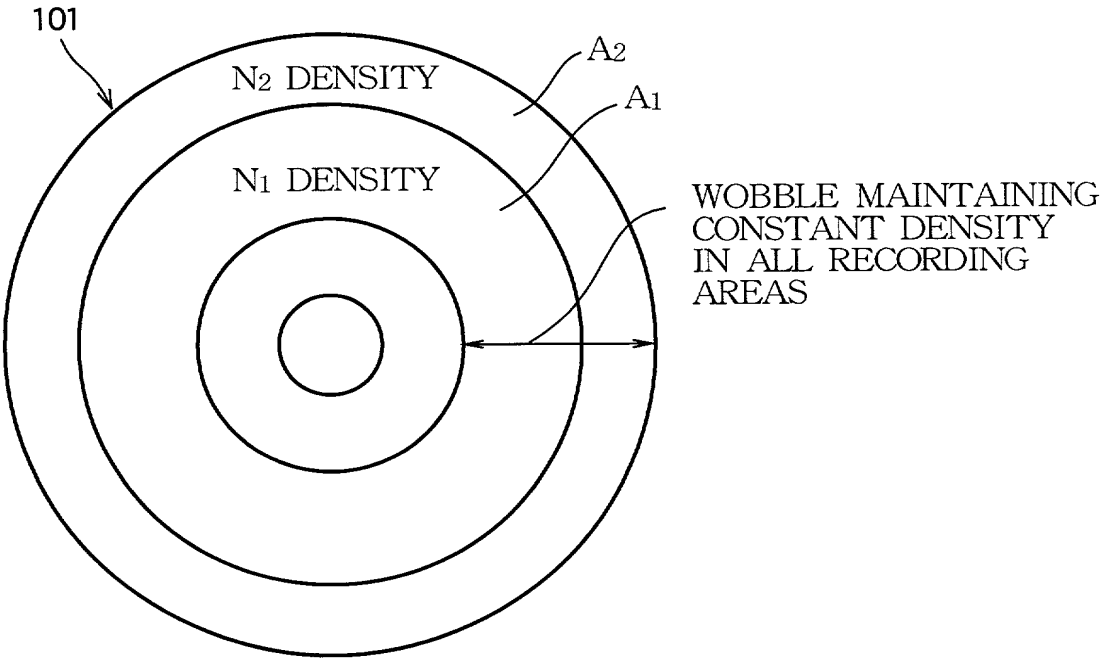
101
N2 DENSITY
A2
A1
N1 DENSITY
WOBBLE MAINTAINING CONSTANT DENSITY IN ALL RECORDING AREAS

FIG.5

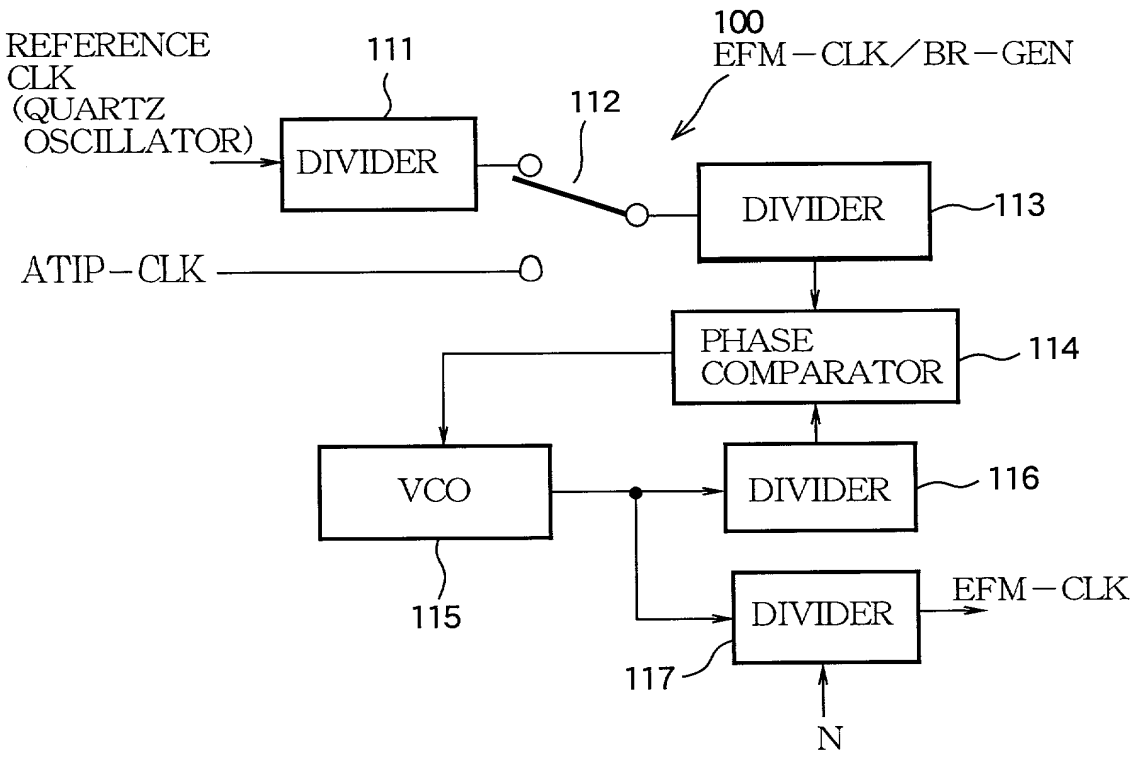
REFERENCE CLK (QUARTZ OSCILLATOR)
111
DIVIDER
112
100
EFM−CLK/BR−GEN
DIVIDER
113
ATIP−CLK
PHASE COMPARATOR
114
VCO
DIVIDER
116
115
DIVIDER
EFM−CLK
117
N

FIG.6

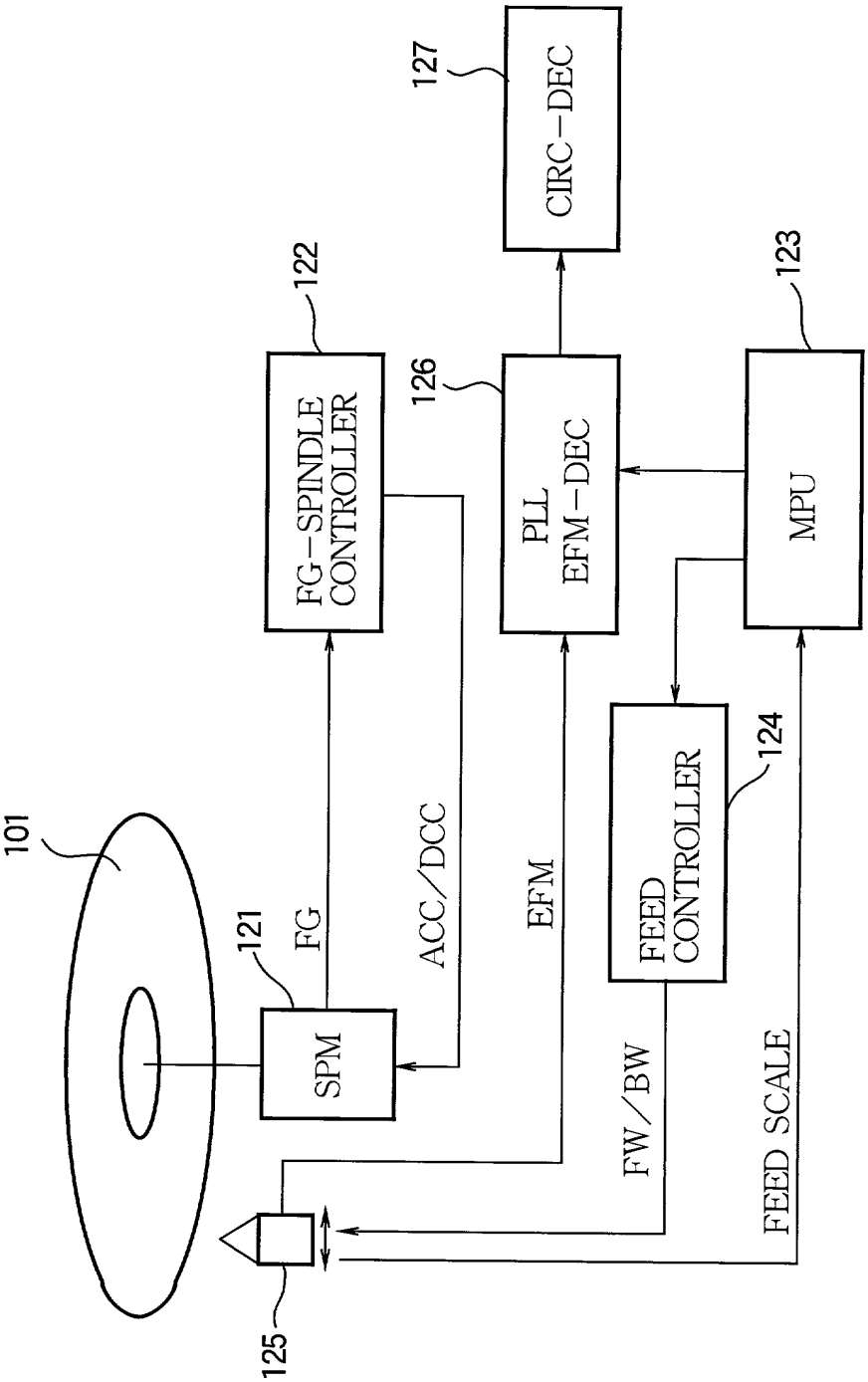
101
121
SPM
FG
ACC/DCC
122
FG-SPINDLE CONTROLLER
125
126
PLL EFM-DEC
EFM
127
CIRC-DEC
123
MPU
124
FEED CONTROLLER
FW/BW
FEED SCALE

FIG. 7

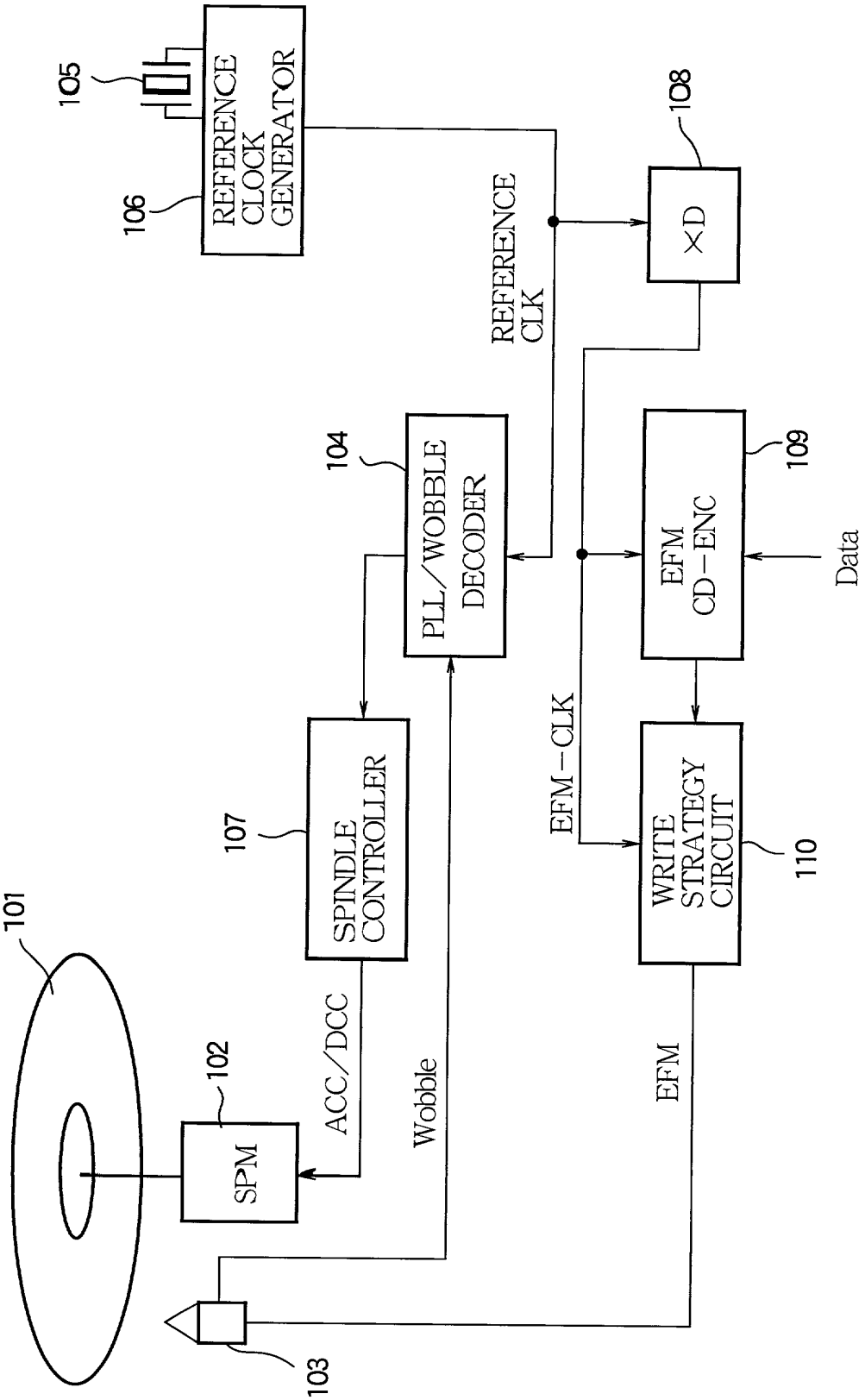
105
106
REFERENCE CLOCK GENERATOR
108
×D
REFERENCE CLK
104
PLL/WOBBLE DECODER
109
EFM CD-ENC
Data
EFM-CLK
107
SPINDLE CONTROLLER
WRITE STRATEGY CIRCUIT
110
101
102
SPM
ACC/DCC
Wobble
EFM
103

FIG. 8

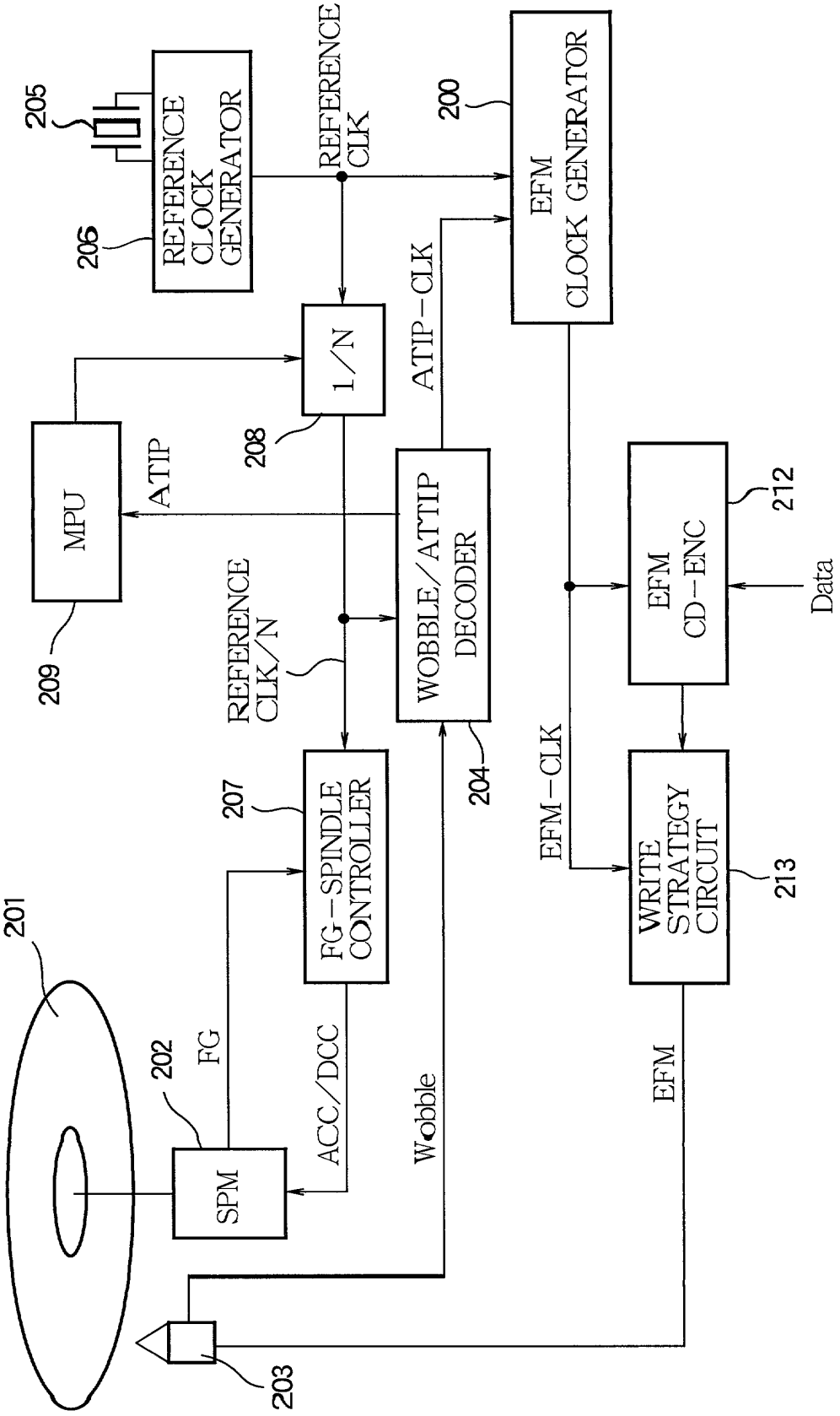
205
206
REFERENCE CLOCK GENERATOR
REFERENCE CLK
200
EFM CLOCK GENERATOR
1/N
208
ATIP-CLK
MPU
ATIP
209
REFERENCE CLK/N
WOBBLE/ATIP DECODER
EFM CD-ENC
212
Data
207
FG-SPINDLE CONTROLLER
204
EFM-CLK
WRITE STRATEGY CIRCUIT
213
201
202
FG
ACC/DCC
Wobble
EFM
SPM
203

FIG.9

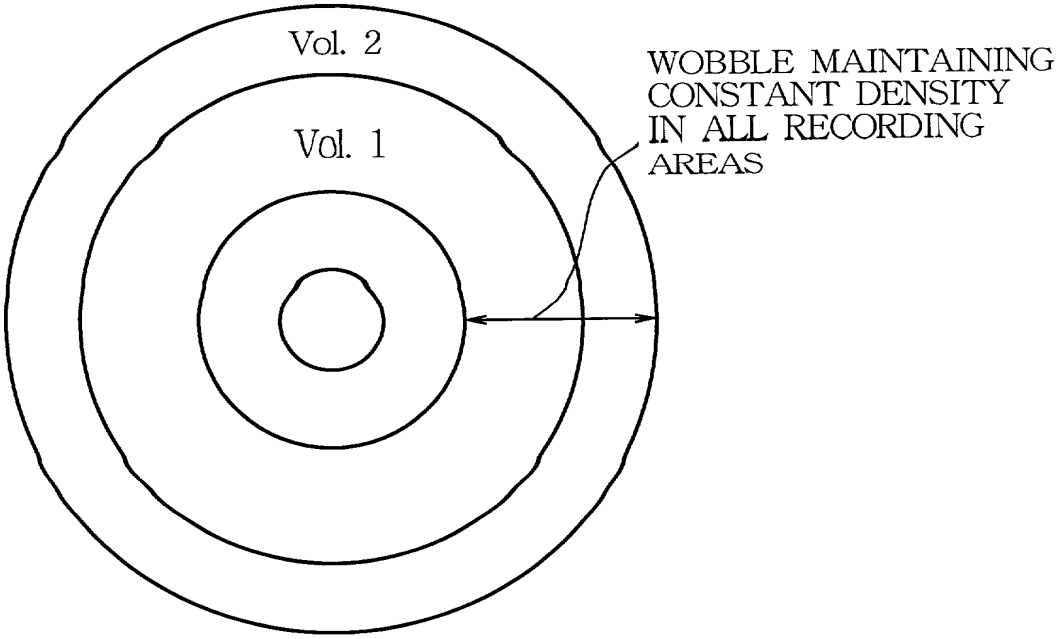

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FIG.10 (a)

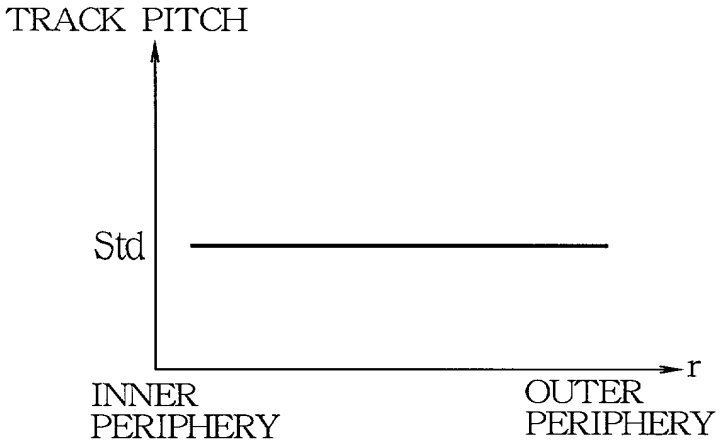

FIG.10 (b)

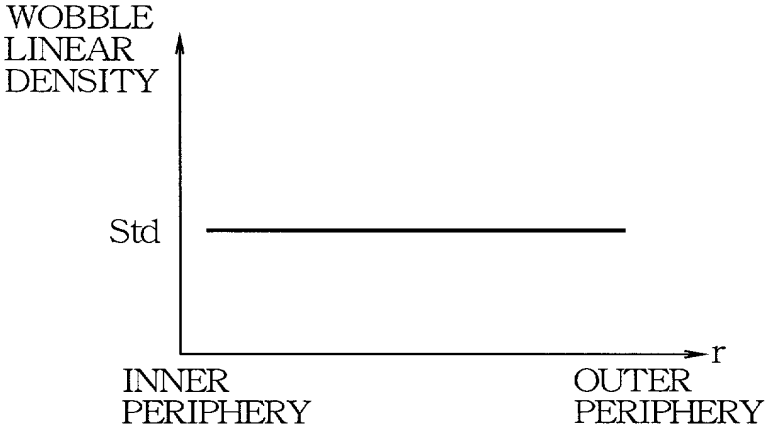

FIG.10 (c)

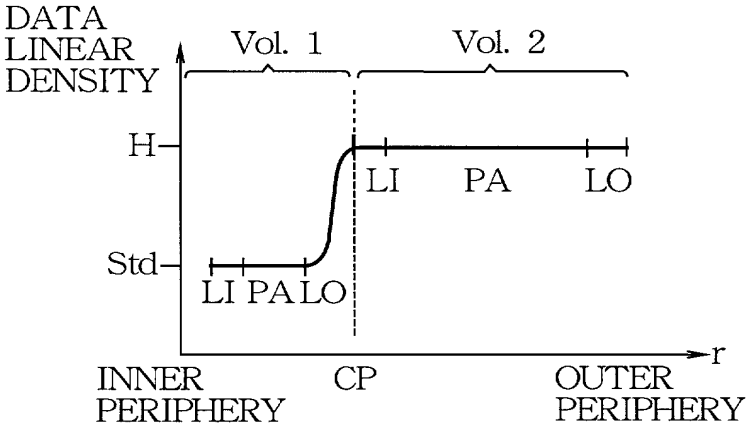

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FIG.11

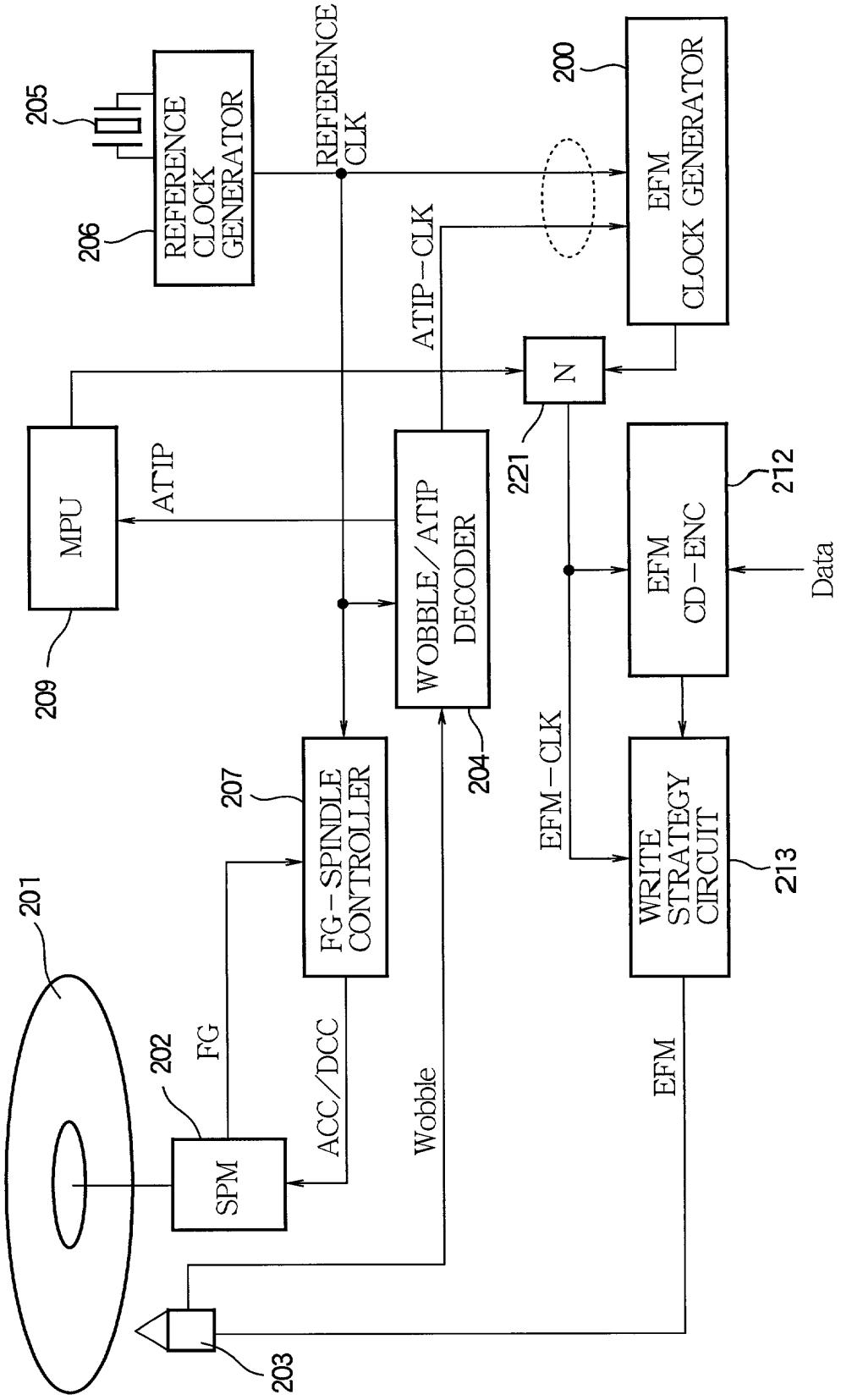
201
202
FG
SPM
ACC/DCC
203
FG-SPINDLE CONTROLLER
207
Wobble
WOBBLE/ATIP DECODER
204
ATIP
MPU
209
ATIP-CLK
REFERENCE CLK
205
206
REFERENCE CLOCK GENERATOR
200
EFM CLOCK GENERATOR
N
221
EFM-CLK
EFM CD-ENC
212
Data
WRITE STRATEGY CIRCUIT
213
EFM

FIG.12 (a)

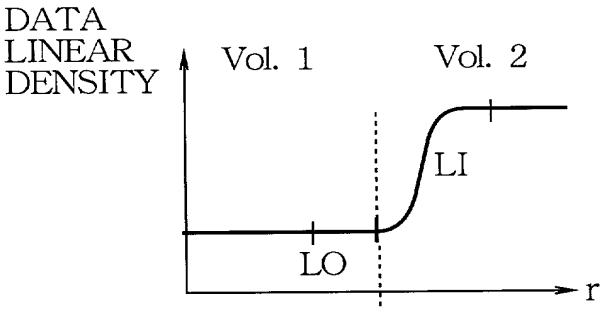

FIG.12 (b)

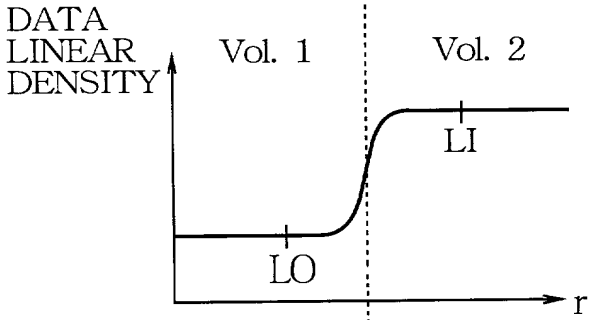

FIG.12 (c)

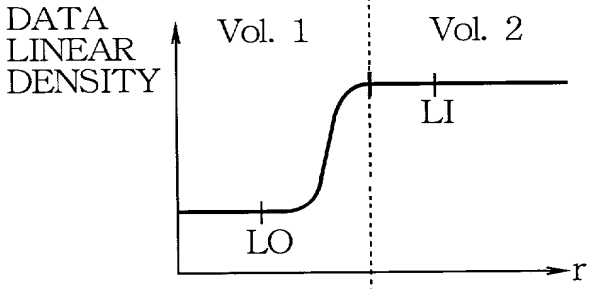

FIG.12 (d)

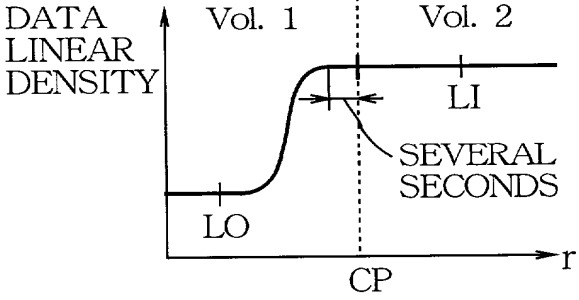

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FIG.13 (a)

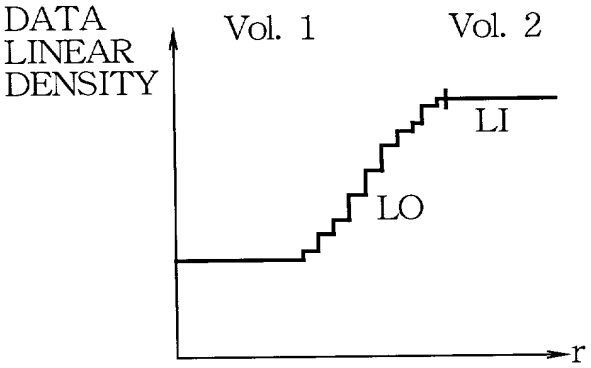


FIG.13 (b)

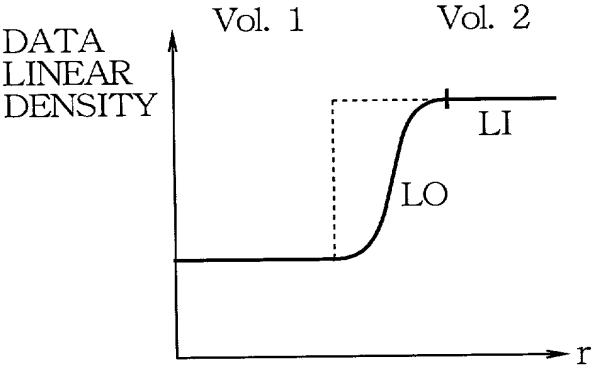
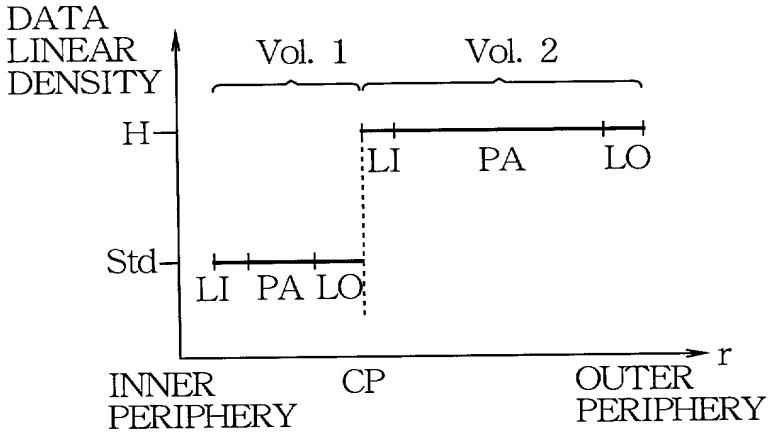


FIG.14



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